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Application Number	10/644,225
Filing Date	August 19, 2003
First Named Inventor	Igor Keller
Art Unit	Unknown
Examiner Name	Unknown
Attorney Docket No.	CA7017522001

U.S. PATENT DOCUMENTS

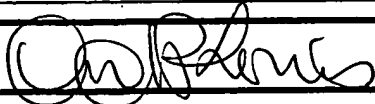
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NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	T ²
APL		L. McMurchie and C. Sechen. WTA - Waveform-Based Timing Analysis for Deep Submicron Circuits. In <i>Proc. IEEE/ACM International Conference on Computer-Aided Design, 2002</i>	
APL		N.H.E. Weste and K. Eshraghian, "Principles of CMOS VLSI Design," 2 nd edition, pages 442-446, 469-471, 645-653, Addison-Wesley Publishing Company 1993	
APL		J. Qian, S. Pullela, and L.T. Pillage, "Modeling the 'Effective Capacitance' for the RC Interconnect of CMOS Gates," <i>IEEE Transactions on CAD</i> , vol. 13, No. 12, pp. 1526-1535.	

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